IN THE SPECIFICATION:

Kindly amend the thirteen continuous paragraphs starting at page 1, line 7 and continuing to page 2, line 15 as shown below.

--U.S. Patent Application Ser. No. 09/652,644 [(15311-2281)] entitled ADAPTIVE DATA PREFETCH PREDICTION ALGORITHM;

U.S. Patent Application Ser. No. 09/653,133 [(15311-2282)] entitled UNIQUE METHOD OF REDUCING LOSSES IN CIRCUITS USING V^2 PWM CONTROL;

U.S. Patent Application Ser. No. 09/652,641 [(15311-2283)] entitled IO SPEED AND LENGTH PROGRAMMABLE WITH BUS POPULATION;

U.S. Patent Application Ser. No. 09/652,458 [(15311-2284)] entitled PARTITION FORMATION USING MICROPROCESSORS IN A MULTIPROCESSOR COMPUTER SYSTEM;

U.S. Provisional Patent Application Ser. No. 60/304,167 [(15311-2285)] entitled SYSTEM AND METHOD FOR USING FUNCTION NUMBERS TO INCREASE THE COUNT OF OUTSTANDING SPLIT TRANSACTIONS;

U.S. Patent Application Ser. No. 09/652,984 [(15311-2286)] entitled SYSTEM AND METHOD FOR PROVIDING FORWARD PROGRESS AND AVOIDING STARVATION AND LIVELOCK IN A MULTIPROCESSOR COMPUTER SYSTEM;

U.S. Patent Application Ser. No. 09/653,180 [(15311-2287)] entitled ONLINE ADD/REMOVAL OF SERVER MANAGEMENT INFRASTRUCTURE;

U.S. Patent Application Ser. No. 09/652,494 [(15311-2288)] entitled AUTOMATED BACKPLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD;

~~U.S. Patent Application Ser. No. (15311-2289) entitled AUTOMATED BACK-PLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD;~~

U.S. Patent Application Ser. No. 09/652,980 [(15311-2290)] entitled CLOCK FORWARD INITIALIZATION AND RESET SIGNALING TECHNIQUE;

U.S. Patent Application Ser. No. 09/944,515 [(15311-2292)] entitled PASSIVE RELEASE AVOIDANCE TECHNIQUE;

A1 cont'd

U.S. Patent Application Ser. No. 09/652,985 [(15311-2293)] entitled COHERENT TRANSLATION LOOK-ASIDE BUFFER;

U.S. Patent Application Ser. No. 09/652,645 [(15311-2294)] entitled DETERMINISTIC HARDWARE BEHAVIOR BETWEEN MULTIPLE ASYNCHRONOUS CLOCK DOMAINS THROUGH THE NOVEL USE OF A PLL; and

U.S. Patent Application Ser. No. 09/655,171 [(15311-2306)] entitled VIRTUAL TIME OF YEAR CLOCK.--

On page 4 of the application, please amend the two full paragraphs in the "Summary of the Invention" section as shown below.

—The present invention generates a phase and edge aligned local clock signal in the data-receiving unit by deriving it from the forwarded clock signal from the transmitting unit.[[.]] Transfers from the input latch to other components in the receiving unit can be thus effected in step with the receipt of data in the input latch. Specifically, data can be transferred from the input latch after it has been loaded therein and before receipt of the next data transmission. For example, if the data is clocked into the input latch on positive-going edges of the clock signal, it can be transferred out of the input latch on negative going edges. This eliminates the latency incurred with the use of FIFO buffers, while insuring the validity of the data passed to other components in the receiving unit.

A2 cont

A9 concl

The invention is particularly applicable to double-data-rate transfers, in which a pair of input latches are loaded with data on alternate transitions of the forwarded clock signal. That is, one latch is loaded on positive-going edges and the second on negative-going edges. As described below, a slight delay is imposed in the transfer of data from one of the latches to a third latch that receives the concatenated data of the two input latches.—

At the top of page 5, please amend the paragraph in the "Brief Description of the Drawings" section as shown below.

A3

—The invention description below refers to the accompanying ~~drawings~~ drawing which is a diagram of a data-receiving unit incorporating the invention.—

On page 5 of the application, please amend the first two full paragraphs in the "Detailed Description of an Illustrative Embodiment" section as shown below.

A4 cont

— ~~In drawing I have illustrated~~ Fig. 1 illustrates the use of the invention in transmitting data from a central processor unit (CPU) 10 [and] to a data unit 12. The units 10 and 12 are parts of a data processing system, which includes other units that need not be depicted for the purposes of this description. The unit 12 may be, for example, an input/output (I/O) ~~I/O~~ Bridge that connects a processor to industry standard busses, such as Peripheral Component Interconnect (PCI), ~~PCI,~~ PCI Extended (PCI-X), ~~PCI-X,~~ Accelerated Graphics Port (AGP) busses, and the like. ~~AGP.~~ It may reside on a separate circuit board from the CPU 10, in which case data transmissions from the CPU to the unit 12 pass over a cable 14. The cable 14 includes a set of data conductors 16 and clock conductors 17 and 18. The conductors 17 and 18 carry a clock signal; the versions on the two conductors being of opposite phase. The CPU 10 transmits data over the data con-

ductors 16 in synchronism with the clock signal. Specifically, whenever a transition in a clock signal is transmitted from the CPU 10, corresponding data is transmitted over the conductors 16. The incoming signals pass through receivers 19.

A4 cont'd

The illustrated system provides for double data-rate transmissions. That is, the CPU 10 transmits data in synchronism with both the positive-going and negative-going ~~transistors~~ transitions of the clock signal. However the invention is applicable also to systems in which the transmissions are synchronized with only the positive-going or negative-going transitions.—

Please amend the paragraph that begins at the bottom of page 5 and carries over to the top of page 6 as shown below.

—For data reception from the CPU 10, the receiving unit 12 includes a pair of input latches 20 and 22 that receive the data transmitted over the cable 14, a pair of latches 24 and 26 that concatenate the data received by the latches 20 and 22, and a phase-lock loop (PLL) 28 that generates a local clock signal for the unit 12. The latches 20 and 22 have data input terminals 20d and 22d that receive the data transmitted over the cable conductor 16. [The] Celock input terminals 20c and 22c on latches 20 and 22 receive delayed versions of the clock signal from delay elements 30 and 32. The elements 30 and 32 preferably provide a delay of 90° ~~to issue~~ to insure that the latches 20 and 22 are clocked after the data voltages have settled. A delay element 34 is interposed in the data input to compensate for delay of the clock signal ~~cause~~ caused by the load imposed by the inputs to which the latter signal is delivered.—

A5

Please amend the first full paragraph on page 6 as shown below.

A6

—The data output of the input latch 20 is applied directly to the data input terminal 24d of the ~~later~~ latch 24.—

Please amend the paragraph that begins at the bottom of page 6 and carries over to the top of page 7 as shown below.

A7

—The delay element 38 is inserted between the output of the input latch 22 and the data input terminal of the latch 26 to deal with the effects of clock jitter, i.e., short term variations in the phase of the local clock relative to that of the forwarded clock signal applied to the ~~latches~~ latch 22. Both of the latches 22 and 26 respond to positive-going CLK edges. If a positive edge of the local clock arrives at the clock input terminal ~~26 c~~ 26c slightly before the arrival of the positive edge of the forwarded clock signal at the terminal 22c, valid data from the input latch 22 will be transferred to the latch ~~2~~ 26. However, if the local clock edge arrives at the terminal 26c subsequent to the arrival of the corresponding edge ~~of~~ at the terminal 22c, the contents of the latch 22 may change before they are be transferred to the latch 26. The delay unit 38 delays the arrival of the change in latch 22 contents at the data input terminal 26d so as to insure that even a slightly late clock edge at the terminal 26c will load the correct data into the latch 26.—